CLAIMS

What is claimed is:

1. A circuit comprising:

a first phase-locked loop circuit including: an off-chip reference clock input, a first set of one or more phase-locked loop clock outputs, and a buffered reference clock output; and

a second phase-locked loop circuit including: an on-chip reference clock input and a second set of one or more phase-locked loop clock outputs;

wherein the buffered reference clock output of the first phase-locked loop circuit is electrically coupled to the on-chip reference clock input of the second phase-locked loop circuit.

2. The circuit of claim 1, wherein the first set of one or more phase-locked loop clock outputs of the first phase-locked loop circuit includes at least two phase-locked loop clock outputs.

3. The circuit of claim 1, further including a buffer internal to the first phase-locked loop circuit, the buffer being electrically connected between the off-chip reference clock input and the buffered reference clock output.

4. The circuit of claim 3, wherein the first phase-locked loop circuit and the second phase-locked loop circuit are predefined library circuits.

5. An application-specific integrated circuit (ASIC) including the circuit of claim 1.

6. The ASIC of claim 5, wherein the first phase-locked loop circuit and the second phase-locked loop circuit are predefined library circuits.

7. The circuit of claim 1, wherein the first phase-locked loop circuit and the second phase-locked loop circuit are predefined library circuits.

8. The circuit of claim 1, wherein the off-chip reference clock input of the first phase-locked loop circuit is directly electrically coupled to a pad of a chip.

9. A circuit for receiving an external clock input to generate a first internal clock signal and a second internal clock signal, the circuit comprising:

a first phase-locked loop circuit means including an off-chip reference clock input, a first set of one or more phase-locked loop clock outputs, a buffered reference clock output, and means for buffering a received off-chip reference clock signal electrically coupled between the off-chip reference clock input and the buffered reference clock output; and

a second phase-locked loop circuit means including an on-chip reference clock input and a second set of one or more phase locked loop clock outputs;

wherein the buffered reference clock output of the first phase-locked loop circuit means is electrically coupled to the on-chip reference clock input of the second phase-locked loop circuit means.

10. The circuit of claim 9, wherein the first set of one or more phase-locked loop clock outputs of the first phase-locked loop circuit means includes at least two phase-locked loop clock outputs.

11. The circuit of claim 9, wherein the first phase-locked loop circuit means and the second phase-locked loop circuit means are predefined library circuits.

12. An application-specific integrated circuit (ASIC) including the circuit of claim 9.

13. The ASIC of claim 12, wherein the first phase-locked loop circuit means and the second phase-locked loop circuit means are predefined library circuits.

14. The circuit of claim 9, wherein the off-chip reference clock input of the first phase-locked loop circuit means is directly electrically coupled to a pad of a chip.

15. A method of designing a circuit for generating a first and a second clock reference signals, the method comprising:

selecting a first phase-locked loop macro including an off-chip reference clock input, a first set of one or more phase-locked loop clock outputs, and a buffered reference clock output;

selecting a second phase-locked loop macro including an on-chip reference clock input and a second set of one or more phase locked loop clock outputs; and

connecting the buffered reference clock output of the first phase-locked loop macro to the on-chip reference clock input of the second phase-locked loop macro.

16. The method of claim 15, wherein the circuit is included in an application-specific integrated circuit (ASIC).

17. The method of claim 15, wherein the first phase-locked loop macro includes a buffer connected between the off-chip reference clock input and the buffered reference clock output.

18. A method of generating a first and a second sets of internal clock reference signals on a chip, the method comprising:

receiving, by a first phase-locked loop circuit, an off-chip clock signal;

generating, by the first phase-locked loop circuit, a buffered reference clock signal and the first set of internal clock reference signals;

receiving, by a second phase-locked loop circuit, the buffered reference clock signal; and

generating, by the second phase-locked loop circuit, the second set of internal clock reference signals.

19. The method of claim 18, wherein the chip includes an application-specific integrated circuit (ASIC).

20. A system for generating a first and a second sets of internal clock reference signals on a chip, the system comprising:

means for receiving, by a first phase-locked loop circuit, an off-chip clock signal;

means for generating, by the first phase-locked loop circuit, a buffered reference clock signal and the first set of internal clock reference signals;

means for receiving, by a second phase-locked loop circuit, the buffered reference clock signal; and

means for generating, by the second phase-locked loop circuit, the second set of internal clock reference signals.